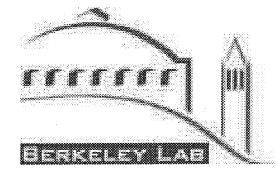


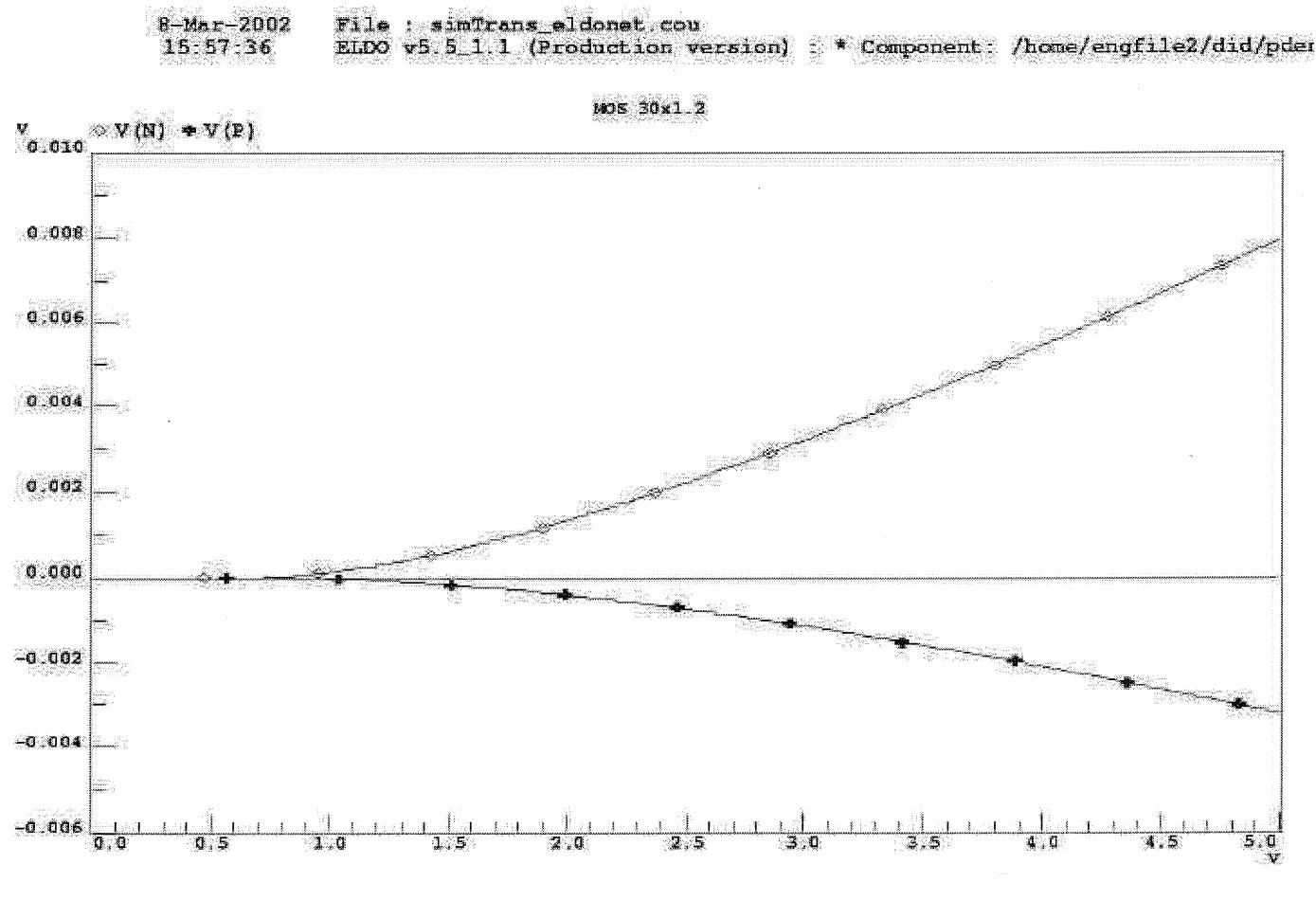
# MOS Level 3 Models from Orbit 1.2 $\mu$ Data

```
.MODEL NCH NMOS LEVEL=3 PHI=0.700000 TOX=2.3500E-08 XJ=0.200000U TPG=1
+ VTO=0.9009 DELTA=1.2610E+00 LD=1.0570E-07 KP=8.3933E-05
+ UO=571.2 THETA=1.1510E-01 RSH=2.7780E+01 GAMMA=0.8699
+ NSUB=4.9220E+16 NFS=9.0900E+10 VMAX=1.9200E+05 ETA=6.9010E-02
+ KAPPA=1.8820E-02 CGDO=2.3298E-10 CGSO=2.3298E-10
+ CGBO=2.6519E-10 CJ=4.88E-04 MJ=0.438 CJSW=4.75E-10
+ MJSW=0.542 PB=0.7
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0000E-09
.MODEL PCH PMOS LEVEL=3 PHI=0.700000 TOX=2.3500E-08 XJ=0.200000U TPG=-1
+ VTO=-0.9596 DELTA=1.6170E+00 LD=9.2210E-10 KP=2.4201E-05
+ UO=164.7 THETA=1.0940E-01 RSH=1.7620E+02 GAMMA=0.4681
+ NSUB=1.4250E+16 NFS=7.1480E+11 VMAX=3.9680E+05 ETA=1.5440E-01
+ KAPPA=7.9050E+00 CGDO=2.0324E-10 CGSO=2.0324E-10
+ CGBO=2.9999E-10 CJ=4.50E-04 MJ=0.511 CJSW=4.15E-10
+ MJSW=0.299 PB=0.9
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 1.0214E-07
```

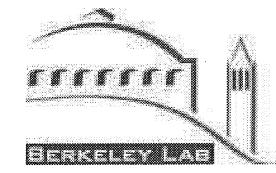
**Charge injection not correctly modeled by MOS Level 3**



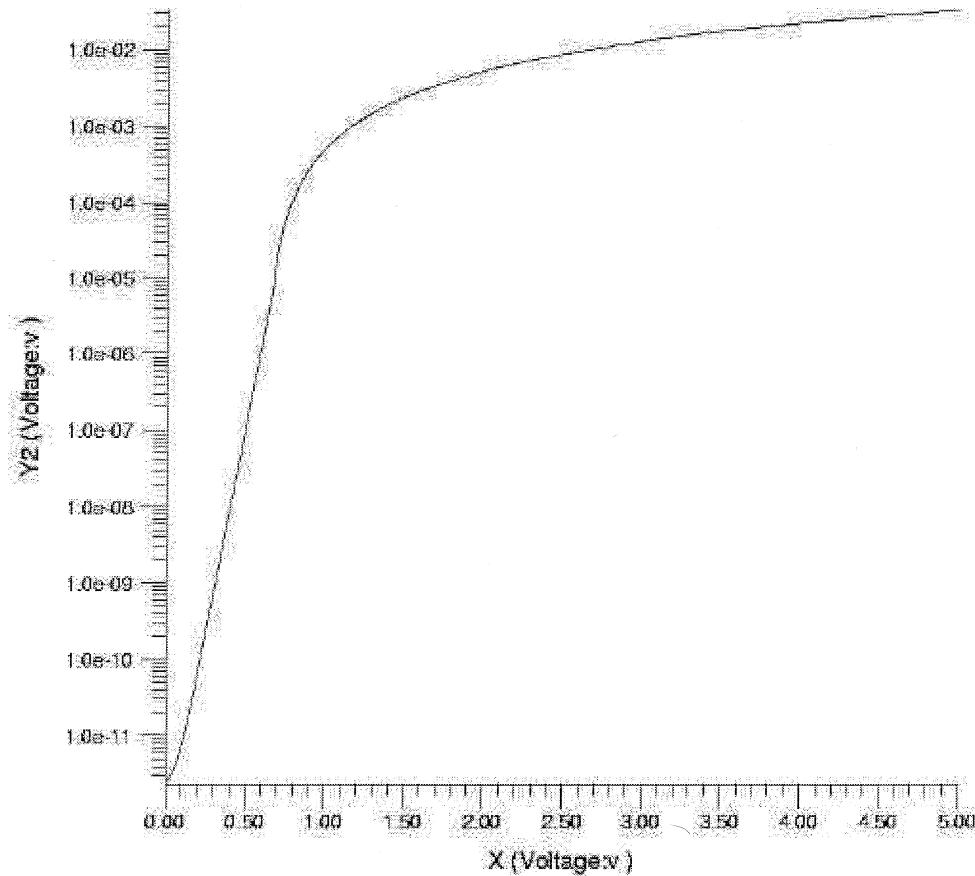
# MOS 30 $\mu$ /1.2 $\mu$



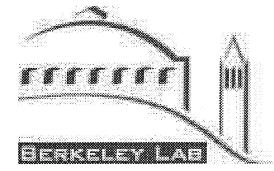
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# NMOS $120\mu/1.2\mu$ - Subthreshold



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# Supertex Design Rule (Nominal) vs. Model

For comparison, selected electrical parameters from Supertex (for the 1.2m Orbit process) are

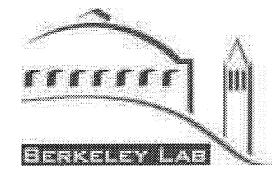
## 1.2 MICRON DOUBLE POLY, DOUBLE METALTWIN-WELL CMOS PROCESS DESIGN RULE

	N-Channel			P-Channel			
	Min	Typ	Max	Min	Typ	Max	
V <sub>TE</sub> (V <sub>BS</sub> =0) 30x1.2μ	0.6	0.8	1.1	-1.1	-0.8	-0.6	(volts)
BVDSS (V <sub>BS</sub> =0) 30x1.2μ	10	13		-13	-10		(volts)
I <sub>DS</sub> @ V <sub>GS</sub> =5v, VDS=5v, L=1.2μ	0.17	0.24	0.29	-0.14	-0.11	-0.08	(mA/micron)
K Prime (Linear) 30x30μ	30	33	36	7.5	9.5	11.5	(μA/V**2)
(k' (linear) = μC <sub>ox</sub> /2)							

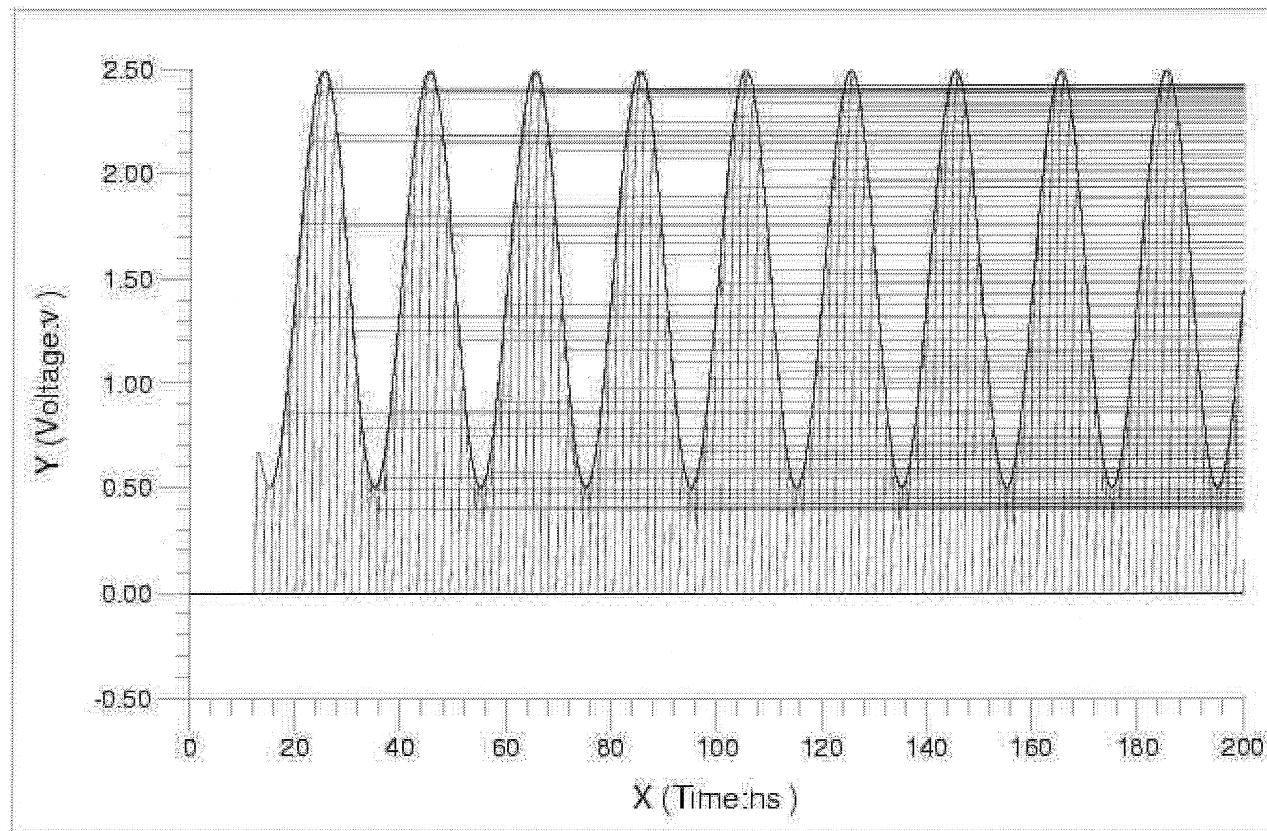
Comparison of the simulation/simulation model (“Simu”) and the Supertex nominal process data (“Spec”) then give

	N-Channel		P-Channel		
	Simu	Spec	Simu	Spec	
VTE (VBS=0) 30x1.2μ	0.9	0.8	-0.96	-0.8	(volts)
IDS @ VGS=5v, VDS=5v, L=1.2μ	0.24	0.24	-0.11	-0.11	(mA/micron)
K Prime (Linear ) 30x30μ	37	33	12	9.5	(μA/V**2)

# Switched Cap Acquisition

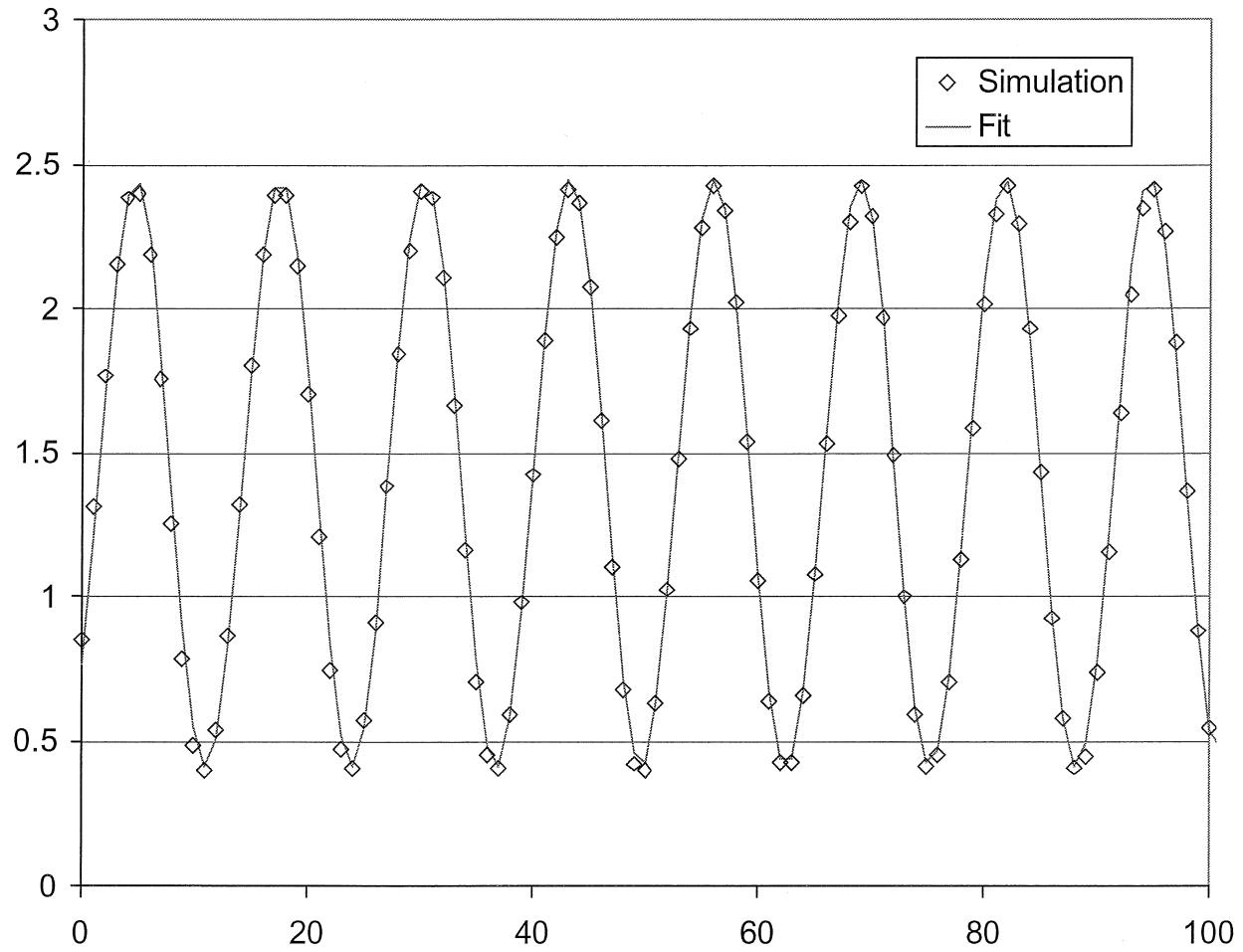
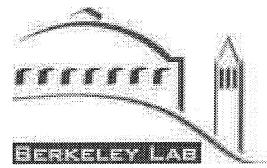


Simulate acquisition of 50 MHz sine wave



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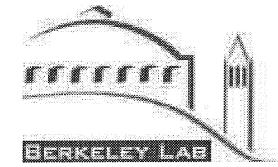
# Switched Cap Acquisition

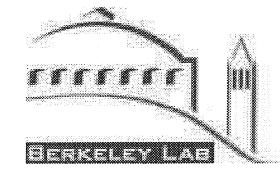


Input:  
1.0V amplitude  
1.5V offset  
50 MHz  
Output:  
 $t_{\text{SAMPLE}} = 1.55 \text{ ns}$   
1.02V amplitude  
1.43V offset

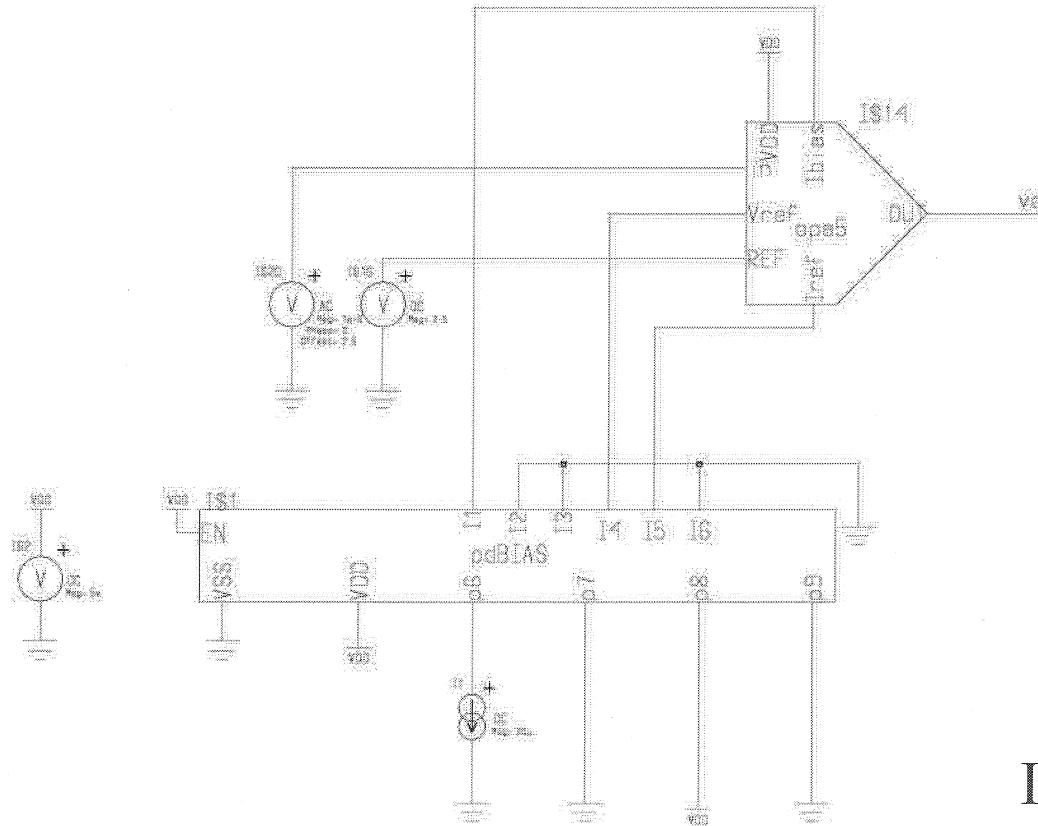
# “Delay Line” $\delta t$ vs. bias

---



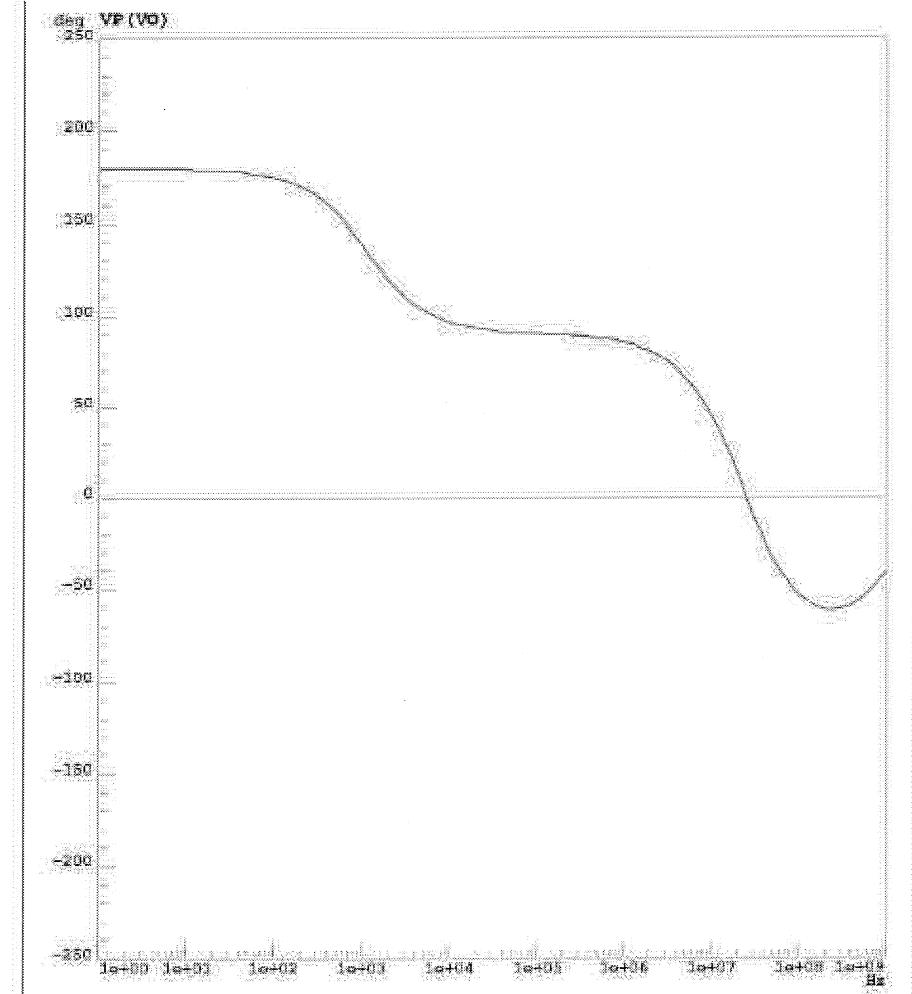
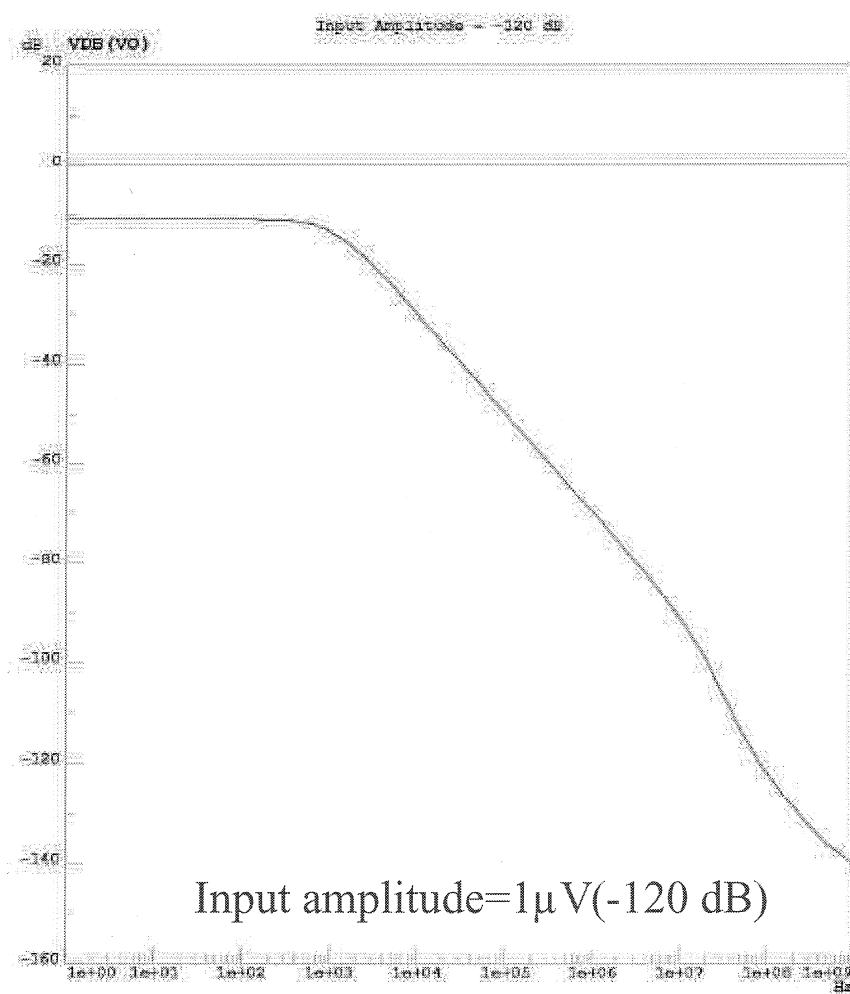
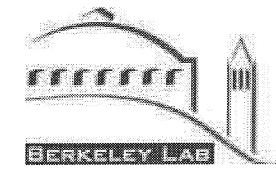


# Simulate OpAmp



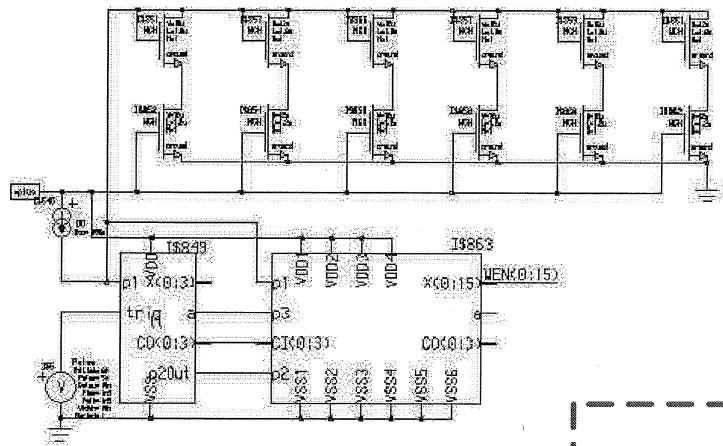
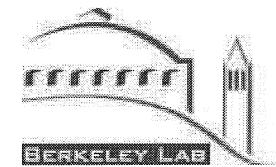
Input amplitude =  $1\mu\text{V}$

# OpAmp Gain&Phase



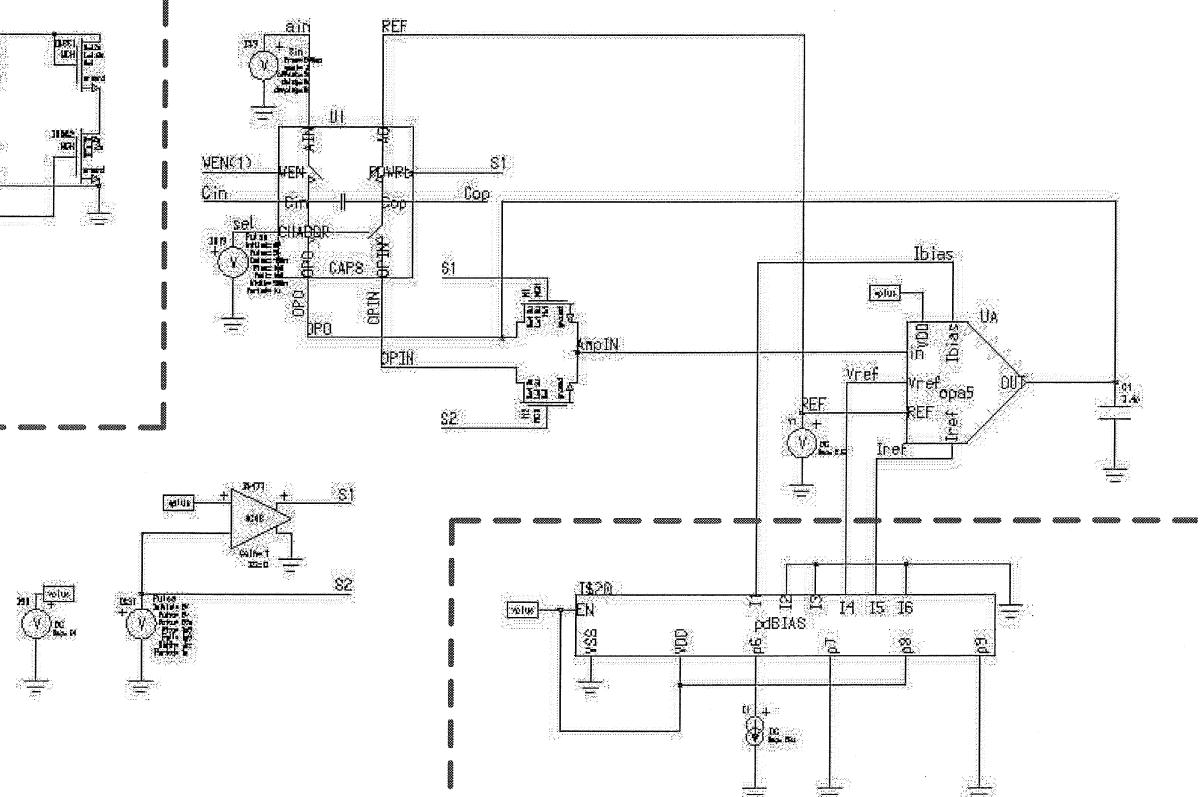
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# Simulate Cap Cell

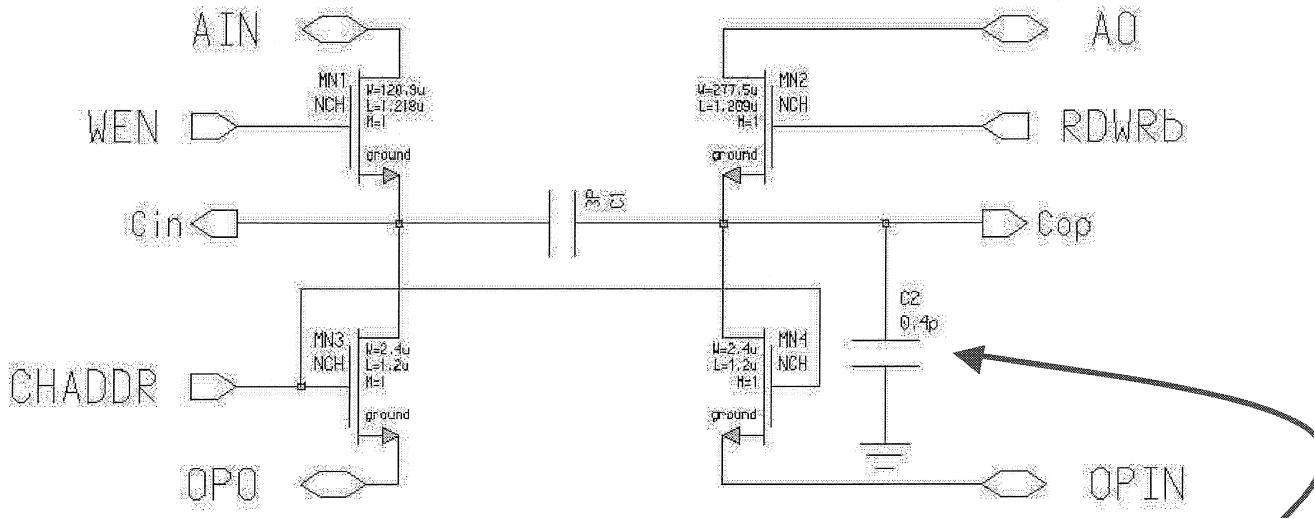
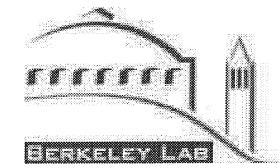


Trigger

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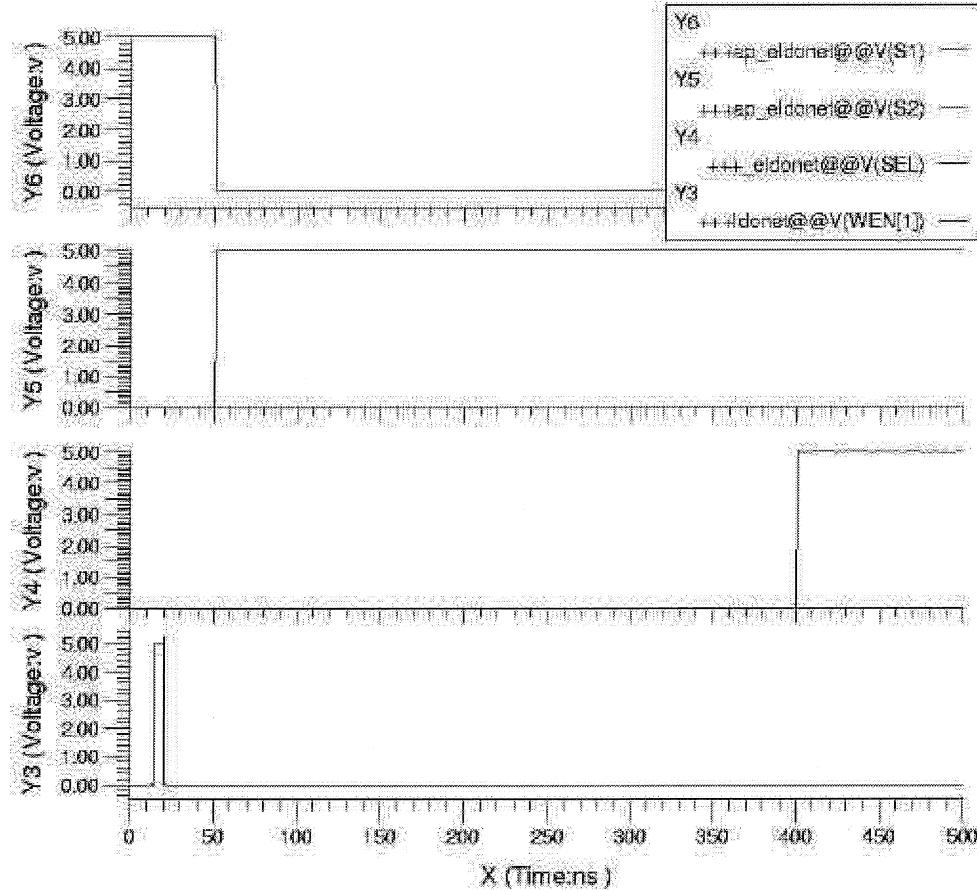
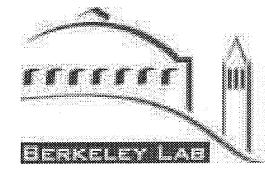


# Note



PIP cap bottom plate-to-substrate capacitance  
Not in *physical* schematic, but important for *simulation*

# Simulation Timing

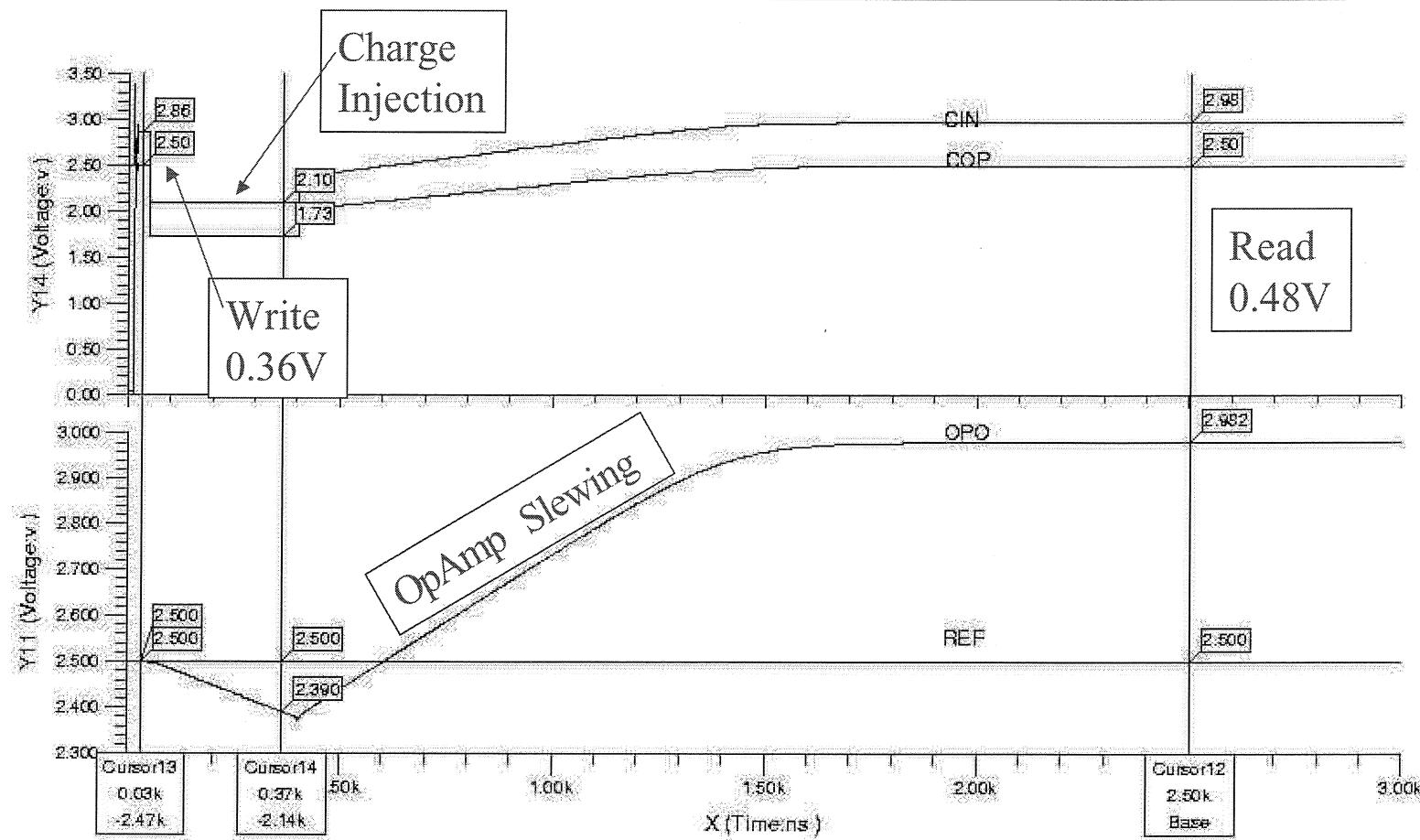
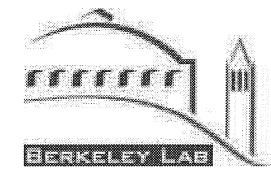


Reset

Read Cap

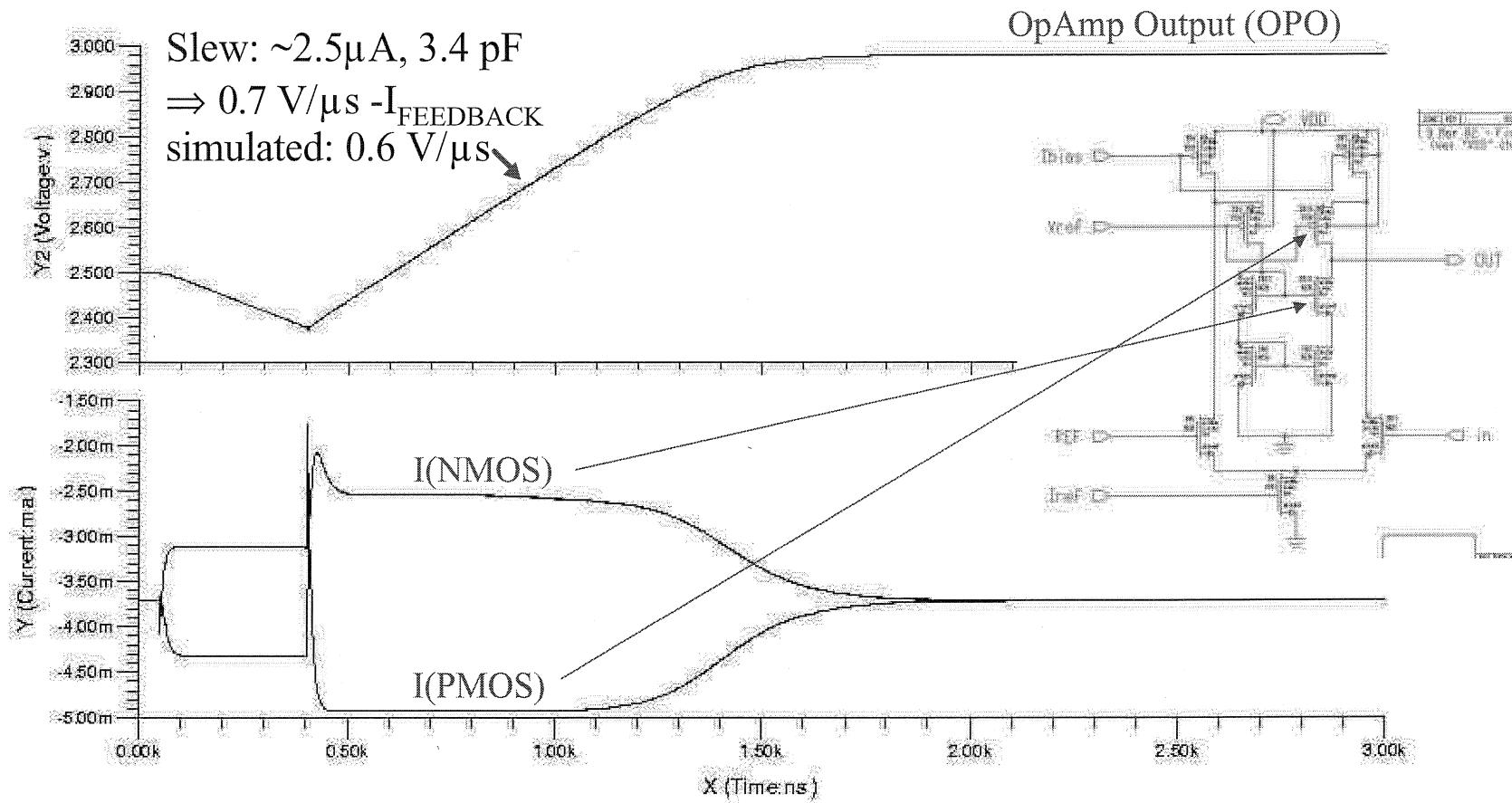
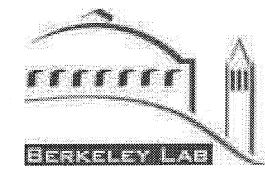
Write Cap

# Cap Cell Behavior

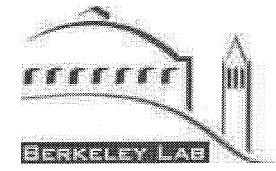


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# OpAmp Slewering

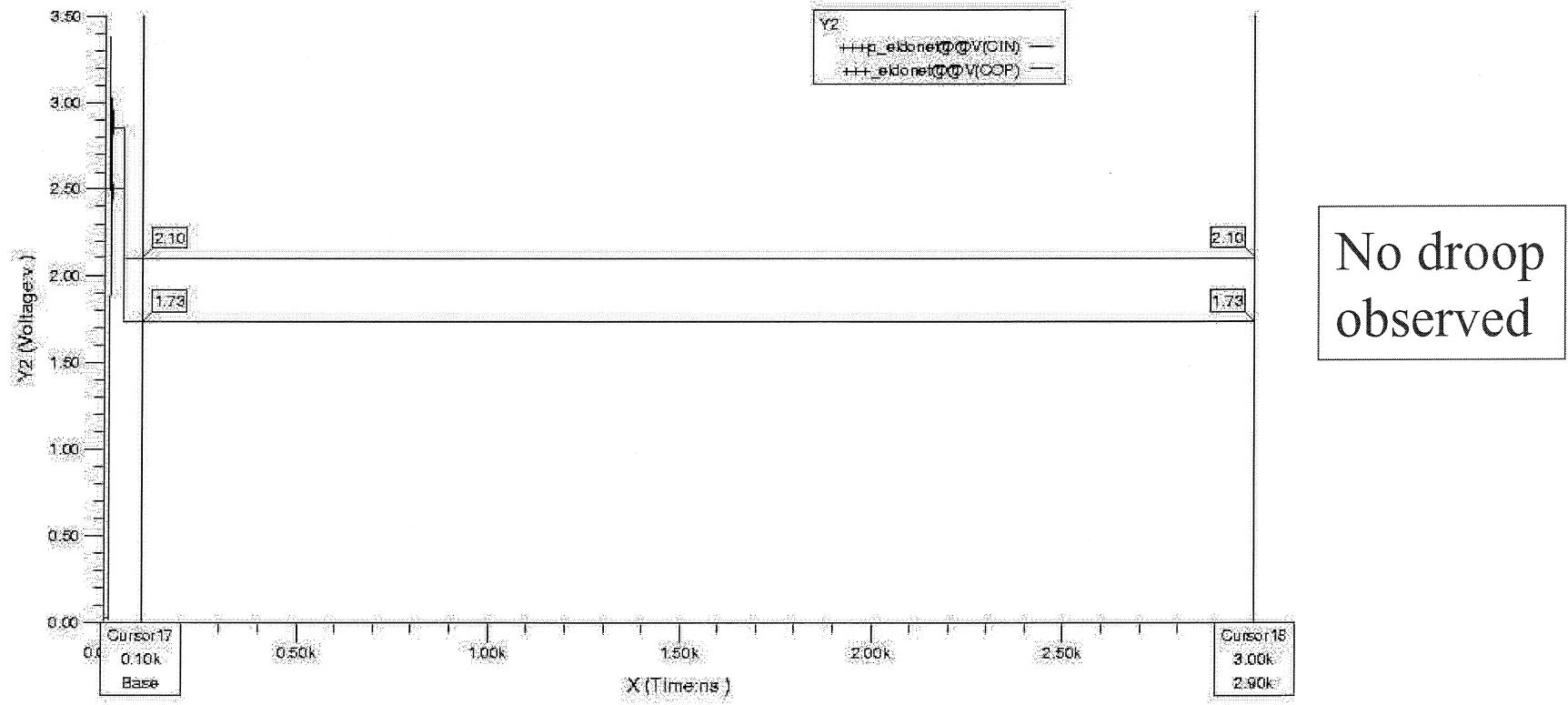


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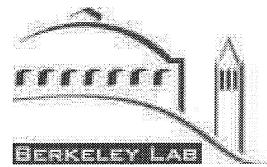


# Droop Rate I.

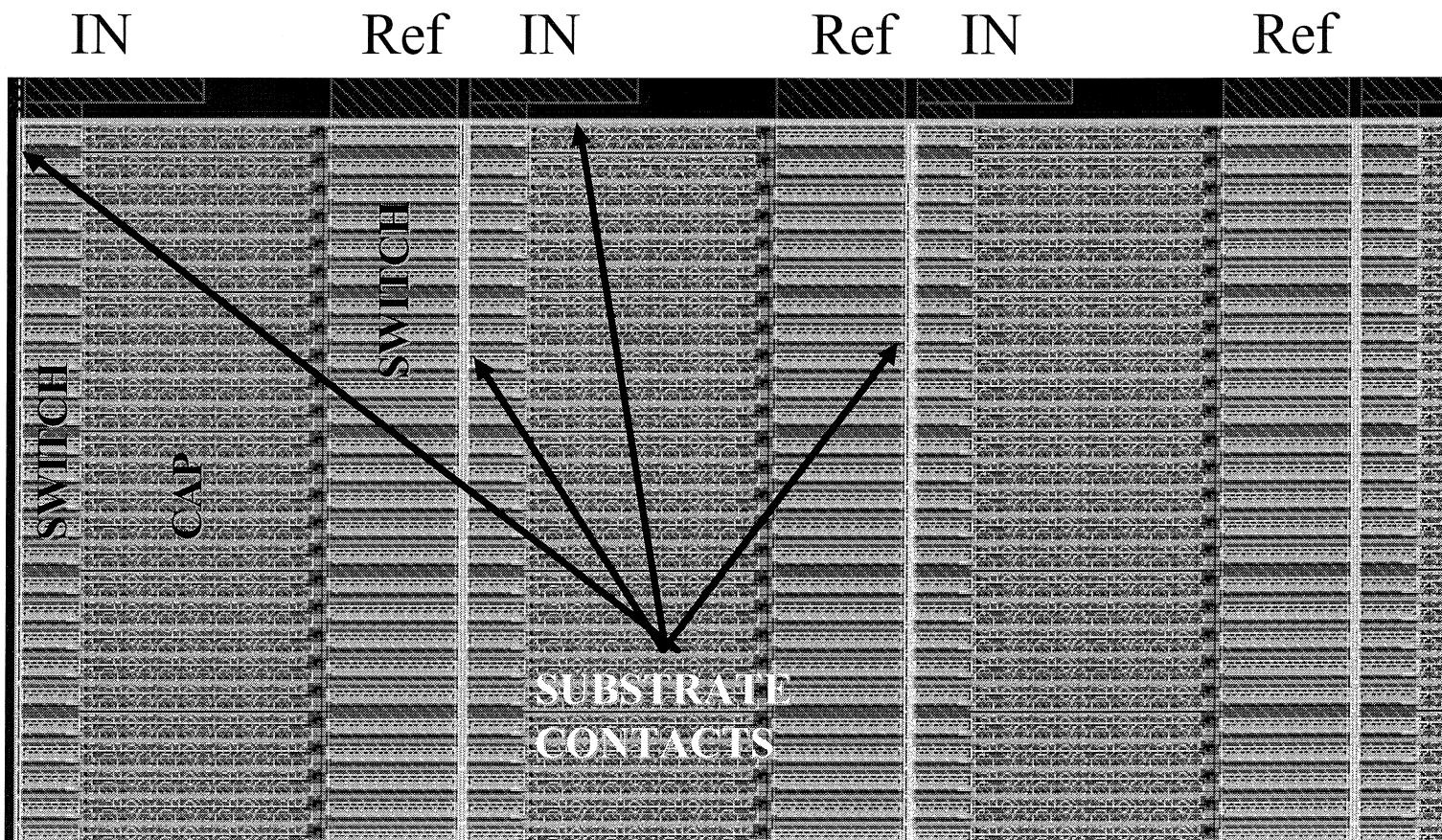
As above, but never “select” cap for readout



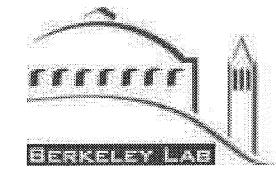
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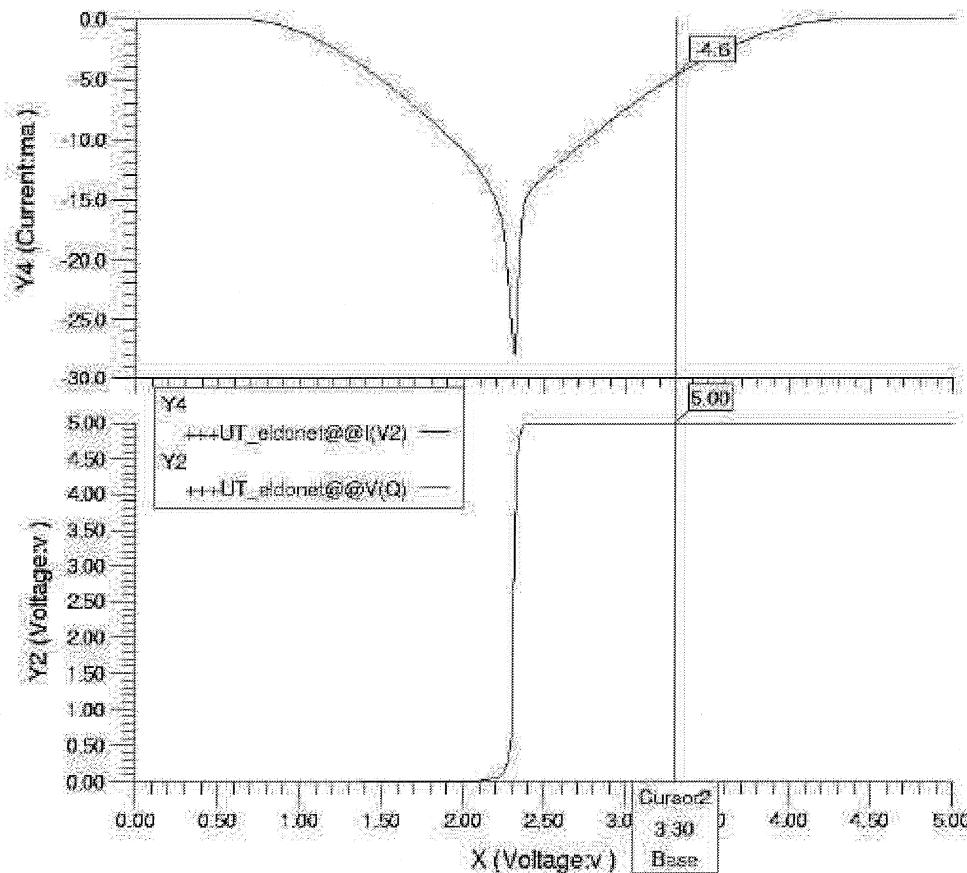
# Switch/Cap layout



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# Input Pad Transfer Function



At 3.3V (nominal)  
current = 4.6 mA  
margin ~1V

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